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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,959	01/28/2002	Chien-chung Hsiao	HSIA3011/EM	2701

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/055,959	Applicant(s) HSIAO ET AL.	
	Examiner Hau H Nguyen	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Brothers, III (U.S. Patent No. 6,128,026).

Referring to claim 1, as cited in admitted prior art, Applicant illustrates in Fig. 1, a graphic engine includes a command queue 10, a setup engine 11, a scan converter 12, a color calculator 13, a texture pipeline unit 14, a depth test unit 15, a memory controller 16, an alpha blending unit 17, and a display controller 18.

Thus, admitted prior art teaches all the limitations of claim 1, except that setup engine perform the validity test.

However, Brothers teaches an accelerator that allows engines to write into a front buffer behind the scan line, wherein as shown in Fig. 3, a method of write blocking accelerator operation begins in step 310 with the SRU 226 drawing to the display 228 using the contents of the front buffer 230A. The SRU 226 preferably reads and outputs display data a scan line at a

time. Concurrent with the activity of the SRU 226, the CPMC 218 processes commands stored in the command queue 216. The presence of a page flip command indicates that the roles of the front and back buffers 230A, 230B are to be reversed. When the CPMC 218 receives or retrieves a page flip command 312 from the command queue 216, the CPMC 218 waits for the currently executing engine 220, or any other engine 220 that might write data into the frame buffer 224, to idle 314, thereby ensuring that the construction of the next image to be displayed has been completed (which implies that the back buffer is full). Next, the CPMC 218 signals the SRU 226 that it has received a page flip command 316. In response, the SRU 226 initializes or sets the values in the last and next address registers 232, 234; signals the MIU 222 to enter write blocking mode; and provides the MIU 222 with the contents of the next address register 234 318. The SRU 226 then continues to transfer display data from the front buffer 230A to the display 228. Each time the SRU 226 reads a line of display data, the SRU 226 preferably increments the next address register's value and transfers the updated next address value to the MIU 222 320. Accordingly, the blocked address range shrinks as the SRU 226 moves or advances through the front buffer 230A. The MIU 222 treats addresses beyond that specified by the next address value (i.e., addresses within the range defined by the contents of the next and last address registers 234, 232) as blocked, into which writes are prohibited. The MIU 222 checks the address ranges of the write requests received from the engines 220 against the next address value received from the SRU 226 (a validity test). Writes to addresses behind the blocked range--that is, writes directed to front buffer addresses for which display data has already been transferred to the display 228--are allowed to proceed 324. Additionally, writes to other parts of the frame buffer 224, such as a Z-buffer, are allowed to proceed (col. 6, lines 19-64).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Brothers in combination with admitted prior art in order to maximize the time that the engines are kept running after page flips and before vertical retrace, thereby also maximizing parallelism between the drawing engines' operation and the occurrence of screen refresh (col. 3, lines 44-51).

In regard to claims 2 and 4, admitted prior art teaches a setup engine 11 and an external memory controller 16 as shown in Fig. 1. Brothers teaches a validity test as cited above.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Brothers in combination with admitted prior art to install a validity test unit in the setup engine or in an external memory controller in order to maximize the time that the engines are kept running after page flips and before vertical retrace, thereby also maximizing parallelism between the drawing engines' operation and the occurrence of screen refresh (col. 3, lines 44-51).

Referring to claims 3 and 5, as cited above, with reference to Figs. 2 and 3, Brothers teaches the MIU 222 checks the address ranges of the write requests received from the engines 220 against the next address value received from the SRU 226. Brothers further teaches the SRU 226 includes a last address register 232 and a next address register 234, which are utilized while in write blocking mode. The last address register 232 preferably stores the starting address of the line after the last line within the current front buffer 230A, and the next address register 234 preferably stores the starting address of the data corresponding to the next scan line to be displayed (col. 6, lines 1-7). Thus, if the primitive lies inside this blocked range (i.e., the Y-

coordinate of the current scan line is greater than the maximum Y-coordinate of the primitive), then writes to the front buffer are allowed.

Therefore, it would have been obvious to one skilled in the art to utilize the method of validity test as taught by Brothers in combination with admitted prior art in order to maximize the time that the engines are kept running after page flips and before vertical retrace, thereby also maximizing parallelism between the drawing engines' operation and the occurrence of screen refresh (col. 3, lines 44-51).

4. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brothers, III (U.S. Patent No. 6,128,026) in view of Derby et al. (U.S. Patent No. 5,761,400).

Referring to claims 6 and 8, as cited above, Brothers teaches a method for writing to the front buffer when the back buffer is full, comprising reading commands from the command queue 216, and determining writing in the front buffer or the back buffer, and performing a validity test in the front buffer for primitives in the blocked address range. Thus, Brothers teach all the limitations of claim 6, except for testing overlapping of primitives.

However, Derby et al. teach a method for removing hidden surfaces of a plurality of overlapping polygons where each one of the plurality polygons is represented by a plurality of scan-lines of points, wherein each one of the points includes a intensity value and a depth value. The method comprises the steps of processing each one of the plurality of polygons one scan-line at a time, wherein the scan-line currently being processed is the current scan-line. A plurality of visible points in the current scan-line are processed separately from a plurality of obscured points in the current scan-line. The processing of the plurality of visible points is controlled using a first sentinel, and the processing of the plurality of obscured points is controlled using a second

sentinel, wherein changes in the intensity values of the plurality of obscured points are not calculated during the processing of the plurality of obscured points (col. 1, lines 60-67, and col. 2, lines 1-9) (testing for overlaps of primitives).

Therefore, it would have been obvious to utilize the method as taught by Derby et al. in combination with the method as taught by Brothers in order to reduce computing time of the z-buffer process, and thereby increasing overall system performance (col. 2, lines 10-13).

In regard to claim 7, as cited above, Brothers teaches the MIU 222 checks the address ranges of the write requests received from the engines 220 against the next address value (the current scan line) received from the SRU 226, and if the primitive lies inside the blocked address range, which means the Y-coordinate of the current scan line is greater than the maximum Y-coordinate of the primitive, then writes to the front buffer are allowed (passes the validity test).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

04/15/2004

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
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